Logic Diagram MCS_CHLC 1-4 0 0 0

1
P04 SOURCE RESISTANCE CRD 0 CHAN0 0
OVERRIDDEN VALUE 0.0
201 COMMON FLOW

2
P04 SOURCE UNUSED 01 NET 0 NODE0 S0
OVERRIDDEN VALUE 0.0
202 BMS CLG RSET

3
P04 SOURCE RESISTANCE CRD 0 CHAN0 0
OVERRIDDEN VALUE 0.0
205 COMMON RET

4
P04 SOURCE UNUSED 01 NET 0 NODE0 S0
OVERRIDDEN VALUE 0.0
206 SPARE

5
P04 SOURCE UNUSED 01 NET 0 NODE0 S0
OVERRIDDEN VALUE 0.0
207 SPARE

6
P04 SOURCE UNUSED 01 NET 0 NODE0 S0
OVERRIDDEN VALUE 0.0
208 SPARE

7
P04 SOURCE UNUSED 01 NET 0 NODE0 S0
OVERRIDDEN VALUE 0.0
210 SPARE

8
P04 SOURCE UNUSED 01 NET 0 NODE0 S0
OVERRIDDEN VALUE 0.0
219 SPARE

9
P04 SOURCE UNUSED 01 NET 0 NODE0 S0
OVERRIDDEN VALUE 0.0
220 SPARE

10
P04 SOURCE UNUSED 01 NET 0 NODE0 S0
OVERRIDDEN VALUE 0.0
221 SPARE

11
P04 SOURCE UNUSED 01 NET 0 NODE0 S0
OVERRIDDEN VALUE 0.0
222 SPARE

12
P04 SOURCE SETPOINT 0 0 0
OVERRIDDEN VALUE 0.0
223 LCHW S.P

13
P04 SOURCE SETPOINT 0 0 0
OVERRIDDEN VALUE 0.0
224 NO OF UNITS

Logic Diagram MCS_CHLC 1-4 0 0 0

14
P04 SOURCE SETPOINT 0 0 0
OVERRIDDEN VALUE 0.0
225 TIM/DEL X100

15
P04 SOURCE SETPOINT 0 0 0
OVERRIDDEN VALUE 0.0
226 CONTROL TYPE

16
P04 SOURCE SETPOINT 0 0 0
OVERRIDDEN VALUE 0.0
227 CLG WTR/BRN

17
P04 SOURCE SETPOINT 0 0 0
OVERRIDDEN VALUE 0.0
228 LOCAL/BMS

18
P04 SOURCE SETPOINT 0 0 0
OVERRIDDEN VALUE 0.0
229 CLG SETPOINT

19
P04 SOURCE SETPOINT 0 0 0
OVERRIDDEN VALUE 0.0
230 CLG C.R

20
P04 SOURCE SETPOINT 0 0 0
OVERRIDDEN VALUE 0.0
231 DTL S.P

21
P04 SOURCE UNUSED 01 NET 0 NODE0 S0
OVERRIDDEN VALUE 1.0
232 U1 UCF RESET

22
P04 SOURCE UNUSED 01 NET 0 NODE0 S0
OVERRIDDEN VALUE 1.0
233 U2 UCF RESET

23
P04 SOURCE UNUSED 01 NET 0 NODE0 S0
OVERRIDDEN VALUE 1.0
234 U3 UCF RESET

24
P04 SOURCE UNUSED 01 NET 0 NODE0 S0
OVERRIDDEN VALUE 1.0
235 U4 UCF RESET

25
P04 SOURCE SETPOINT 0 0 0
OVERRIDDEN VALUE 0.0
236 FLOW/DTL

26
P04 SOURCE SETPOINT 0 0 0
OVERRIDDEN VALUE 0.0
237 PAR/SERIES

Logic Diagram MCS_CHLC 1-4 0 0 0

27

P04 SOURCE SETPOINT 0 0 0 OVERRIDDEN VALUE 0.0	238 FIXED/VAR

28

P04 SOURCE UNUSED 01 NET 0 NODE0 S0 OVERRIDDEN VALUE 0.0	239 CLG_RESET

29

P04 SOURCE CURRENT CRD 0 CHAN0 0 OVERRIDDEN VALUE 0.0	250 COMMON RET 1

30

P04 SOURCE CURRENT CRD 0 CHAN0 0 OVERRIDDEN VALUE 0.0	251 COMMON RET 2

31

Enable when 636 MADE Trigger when 000 MADE	301 CLG ERROR CALCULATION 326-339 / 303 000

32

Enable when 618 MADE Trigger when 000 MADE	302 ICD CALCULATION 000 000 000 000

33

Enable when 636 MADE Trigger when 000 MADE	303 CLG C.R CALCULATION 230*322 000 000

34

Enable when 620 MADE Trigger when 000 MADE	304 RCD CALCULATION 000 000 000 000

35

Enable when 637 MADE Trigger when 635 MADE	305 ICD/RCD TMR CALCULATION 302+304 + 350+305

36

Enable when 000 MADE Trigger when 624 MADE	306 PDR CALC 1 CALCULATION 201 000 000 000

37

Enable when 000 MADE Trigger when 000 MADE	307 PDR CALC 2 CALCULATION 201 000 000 000

38

Enable when 636 MADE Trigger when 000 MADE	308 PDR CALC 3 CALCULATION 307-306 000 000

39

Enable when 642 OPEN Trigger when 000 OPEN	309 RCD SETPOINT CALCULATION 352*211 / 351 000

Logic Diagram MCS_CHLC 1-4 0 0 0

40

Enable when 000 MADE	310 DTL
Trigger when 000 MADE	CALCULATION 392-340 / 312 000

41

Enable when 642 OPEN	311 DTL-RCD
Trigger when 000 OPEN	CALCULATION 310-309 000 000

42

Enable when 000 MADE	312 DTL FACTOR
Trigger when 000 MADE	CALCULATION 212 000 000 000

43

Enable when 000 MADE	313 SEQ CNTL1
Trigger when 000 MADE	CALCULATION 315-316 000 000

44

Enable when 000 MADE	314 SEQ CNTL2
Trigger when 000 MADE	2ND HIGHEST 316 315 000 000

45

Enable when 000 MADE	315 UNITS AVBL
Trigger when 000 MADE	CALCULATION 209-334 000 000

46

Enable when 000 MADE	316 TIME ADJUST
Trigger when 000 MADE	CALCULATION 305/362 000 000

47

Enable when 000 MADE	317 SEQ CNTL3
Trigger when 000 MADE	CALCULATION 314-214 000 000

48

Enable when 647 MADE	318 U1 SER S-PT
Trigger when 000 MADE	CALCULATION 310*312 000 000

49

Enable when 000 MADE	320 TARGETREPORT
Trigger when 000 MADE	CALCULATION 363+901 000 000

50

Enable when 669 OPEN	321 CLG S.P ACT
Trigger when 000 OPEN	CALCULATION 339 000 000 000

51

Enable when 642 OPEN	322 C.R X2
Trigger when 000 OPEN	CALCULATION 203 000 000 000

52

Enable when 000 MADE	323 RCD/TIMAJUST
Trigger when 000 MADE	CALCULATION 316-314 000 000

Logic Diagram MCS_CHLC 1-4 0 0 0

53

Enable when 000 MADE	324 S.T.A.1
Trigger when 000 MADE	CALCULATION 358-326 000 000

54

Enable when 000 MADE	325 S.T.A.2
Trigger when 000 MADE	CALCULATION 204*324 000 000

55

Enable when 000 MADE	326 S.T.A.3
Trigger when 000 MADE	CALCULATION 326+325 000 000

56

Enable when 000 MADE	327 UNIT.1 CALC
Trigger when 000 MADE	CALCULATION 638-643 000 000

57

Enable when 000 MADE	328 UNIT.2 CALC
Trigger when 000 MADE	CALCULATION 639-644 000 000

58

Enable when 000 MADE	329 UNIT.3 CALC
Trigger when 000 MADE	CALCULATION 640-645 000 000

59

Enable when 000 MADE	330 UNIT.4 CALC
Trigger when 000 MADE	CALCULATION 641-646 000 000

60

Enable when 664 MADE	331 CLG S-P LOC
Trigger when 000 MADE	CALCULATION 229 000 000 000

61

Enable when 664 OPEN	332 CLG S-P BMS
Trigger when 000 OPEN	CALCULATION 401 000 000 000

62

Enable when 659 MADE	333 S-PT WTR ENA
Trigger when 000 MADE	CALCULATION 331+332 000 000

63

Enable when 000 MADE	334 U1-4 UNAVBL
Trigger when 000 MADE	CALCULATION 609+610 + 611+612

64

Enable when 000 MADE	335 PULSE CALC.1
Trigger when 000 MADE	CALCULATION 354 000 000 000

65

Enable when 000 MADE	336 PULSE CALC.2
Trigger when 000 MADE	CALCULATION 336-337 000 000

Logic Diagram MCS_CHLC 1-4 0 0 0

66

Enable when 000 MADE	337 PULSE CALC.3
Trigger when 000 MADE	CALCULATION 336-335 000 000

67

Enable when 659 OPEN	338 S-PT BRN ENA
Trigger when 000 OPEN	CALCULATION 331+332 000 000

68

Enable when 000 MADE	339 SETPOINT CLG
Trigger when 000 MADE	CALCULATION 333+338 + 239 000

69

Enable when 000 MADE	340 DTL S.P
Trigger when 000 MADE	CALCULATION 379+380 000 000

70

Enable when 638 MADE	341 U1 UCF
Trigger when 000 MADE	CALCULATION 215*370 000 000

71

Enable when 639 MADE	342 U2 UCF
Trigger when 000 MADE	CALCULATION 216*371 000 000

72

Enable when 640 MADE	343 U3 UCF
Trigger when 000 MADE	CALCULATION 217*372 000 000

73

Enable when 641 MADE	344 U4 UCF
Trigger when 000 MADE	CALCULATION 218*373 000 000

74

Enable when 000 MADE	345 U1 CALC S.P
Trigger when 000 MADE	CALCULATION 363+321 + 712+318

75

Enable when 000 MADE	346 U2 CALC S.P
Trigger when 000 MADE	CALCULATION 363+321 + 713 000

76

Enable when 000 MADE	347 U3 CALC S.P
Trigger when 000 MADE	CALCULATION 363+321 + 714 000

77

Enable when 000 MADE	348 U4 CALC S.P
Trigger when 000 MADE	CALCULATION 363+321 + 715 000

78

Enable when 000 MADE	349 U1-U4 UCF
Trigger when 000 MADE	CALCULATION 341+342 + 343+344

Logic Diagram MCS_CHLC 1-4 0 0 0

79

Enable when 637 OPEN	350 TIME AMMEND
Trigger when 000 OPEN	CALCULATION 362 000 000 000

80

Enable when 000 MADE	351 TOT UCF
Trigger when 000 MADE	CALCULATION 349+000 000 000

81

Enable when 000 MADE	352 TOTAL UCF-1
Trigger when 000 MADE	CALCULATION 369+000 000 000

82

Enable when 000 MADE	353 ACT RUN
Trigger when 000 MADE	CALCULATION 359+000 000 000

83

Enable when 000 MADE	354 UNIT REQ'D
Trigger when 000 MADE	CALCULATION 361+000 000 000

84

Enable when 636 MADE	356 COMMON FLOW
Trigger when 000 MADE	CALCULATION 201 000 000 000

85

Enable when 636 OPEN	357 DTL CONTROL
Trigger when 000 OPEN	CALCULATION 310 000 000 000

86

Enable when 000 MADE	358 CONTROL TYPE
Trigger when 000 MADE	CALCULATION 356+357 000 000

87

Enable when 000 MADE	359 ACTRUN1-4
Trigger when 000 MADE	CALCULATION 650+651 + 652+653

88

Enable when 000 MADE	360 MIN TIME
Trigger when 000 MADE	CALCULATION 305-362 000 000

89

Enable when 000 MADE	361 UNITSREQ1-4
Trigger when 000 MADE	CALCULATION 638+639 + 640+641

90

Enable when 000 MADE	362 TIME DELAY
Trigger when 000 MADE	CALCULATION 225 000 000 000

91

Enable when 669 MADE	363 LCHW S.P
Trigger when 000 MADE	CALCULATION 223 000 000 000

Logic Diagram MCS_CHLC 1-4 0 0 0

92

Enable when 636 OPEN	364 DTL ERROR
Trigger when 000 OPEN	CALCULATION 326-231 / 303 000

93

Enable when 643 MADE	365 U1 UCF -
Trigger when 000 MADE	CALCULATION 341+000 000 000

94

Enable when 644 MADE	366 U2 UCF -
Trigger when 000 MADE	CALCULATION 342+000 000 000

95

Enable when 645 MADE	367 U3 UCF -
Trigger when 000 MADE	CALCULATION 343+000 000 000

96

Enable when 646 MADE	368 U4 UCF -
Trigger when 000 MADE	CALCULATION 344+000 000 000

97

Enable when 000 MADE	369 U1-U4 CAP -
Trigger when 000 MADE	CALCULATION 365+366 + 367+368

98

Enable when 627 MADE	370 U1 UCF RESET
Trigger when 000 MADE	CALCULATION 402 000 000 000

99

Enable when 628 MADE	371 U2 UCF RESET
Trigger when 000 MADE	CALCULATION 403 000 000 000

100

Enable when 629 MADE	372 U3 UCF RESET
Trigger when 000 MADE	CALCULATION 404 000 000 000

101

Enable when 630 MADE	373 U4 UCF RESET
Trigger when 000 MADE	CALCULATION 405 000 000 000

102

Enable when 000 MADE	374 U1 ACT S.P
Trigger when 000 MADE	LOWEST 345 378 000 000

103

Enable when 000 MADE	375 U2 ACT S.P
Trigger when 000 MADE	LOWEST 346 378 000 000

104

Enable when 000 MADE	376 U3 ACT S.P
Trigger when 000 MADE	LOWEST 347 378 000 000

Logic Diagram MCS_CHLC 1-4 0 0 0

105

Enable when 000 MADE	377 U4 ACT S.P
Trigger when 000 MADE	LOWEST 348 378 000 000

106

Enable when 649 MADE	378 VAR HI LIMIT
Trigger when 000 MADE	CALCULATION 339 000 000 000

107

Enable when 649 MADE	379 VARREPORT.1
Trigger when 000 MADE	LOWEST 320 378 000 000

108

Enable when 649 OPEN	380 VARREPORT.2
Trigger when 000 OPEN	CALCULATION 374 000 000 000

109

Enable when 000 MADE	381 S.T.A.1F37
Trigger when 000 MADE	CALCULATION 201-383 000 000

110

Enable when 000 MADE	382 S.T.A.2F37
Trigger when 000 MADE	CALCULATION 204*381 000 000

111

Enable when 000 MADE	383 S.T.A.3F37
Trigger when 000 MADE	CALCULATION 383+382 000 000

112

Enable when 601 MADE	390 COMMON RET 1
Trigger when 000 MADE	CALCULATION 250 000 000 000

113

Enable when 602 MADE	391 COMMON RET 2
Trigger when 000 MADE	CALCULATION 251 000 000 000

114

Enable when 000 MADE	392 COMMON RET
Trigger when 000 MADE	HIGHEST 390 391 000 000

115

P04 SOURCE BACNET LOC 0 MAC 0 +0	401 BMS CLG RSET
OVERRIDDEN VALUE 0.0	

116

P04 SOURCE BACNET LOC 0 MAC 0 +0	402 U1 UCF RESET
OVERRIDDEN VALUE 0.0	

117

P04 SOURCE BACNET LOC 0 MAC 0 +0	403 U2 UCF RESET
OVERRIDDEN VALUE 0.0	

Logic Diagram MCS_CHLC 1-4 0 0 0

118

P03 SOURCE DIGITAL CRD 0 CHAN0 0
DEFAULT STATE OPEN

501 PER TO RUN 1

119

P03 SOURCE DIGITAL CRD 0 CHAN0 0
DEFAULT STATE OPEN

502 PER TO RUN 2

120

P03 SOURCE UNUSED 03 0 0 0
DEFAULT STATE OPEN

516 DIL_CYC.1

121

P03 SOURCE UNUSED 03 0 0 0
DEFAULT STATE OPEN

517 DIL_CYC.2

122

P03 SOURCE UNUSED 03 0 0 0
DEFAULT STATE OPEN

518 DIL_CYC.3

123

P03 SOURCE UNUSED 03 0 0 0
DEFAULT STATE OPEN

519 DIL_CYC.4

124

P03 SOURCE DIGITAL CRD 0 CHAN0 0
DEFAULT STATE OPEN

525 REM SYS REQD

125

Home to 0.0 when 655 MADE

712 UNIT.1 RESET
UNIT.1 RESET

126

Home to 0.0 when 656 MADE

713 UNIT.2 RESET
UNIT.2 RESET

127

Home to 0.0 when 657 MADE

714 UNIT.3 RESET
UNIT.3 RESET

128

Home to 0.0 when 658 MADE

715 UNIT.4 RESET
UNIT.4 RESET

129

Enable when 601 Made
Alarm Master Delay = 200

1209 NOTIFICATION
PER TO RUN 1

130

Enable when 602 Made
Alarm Master Delay = 200

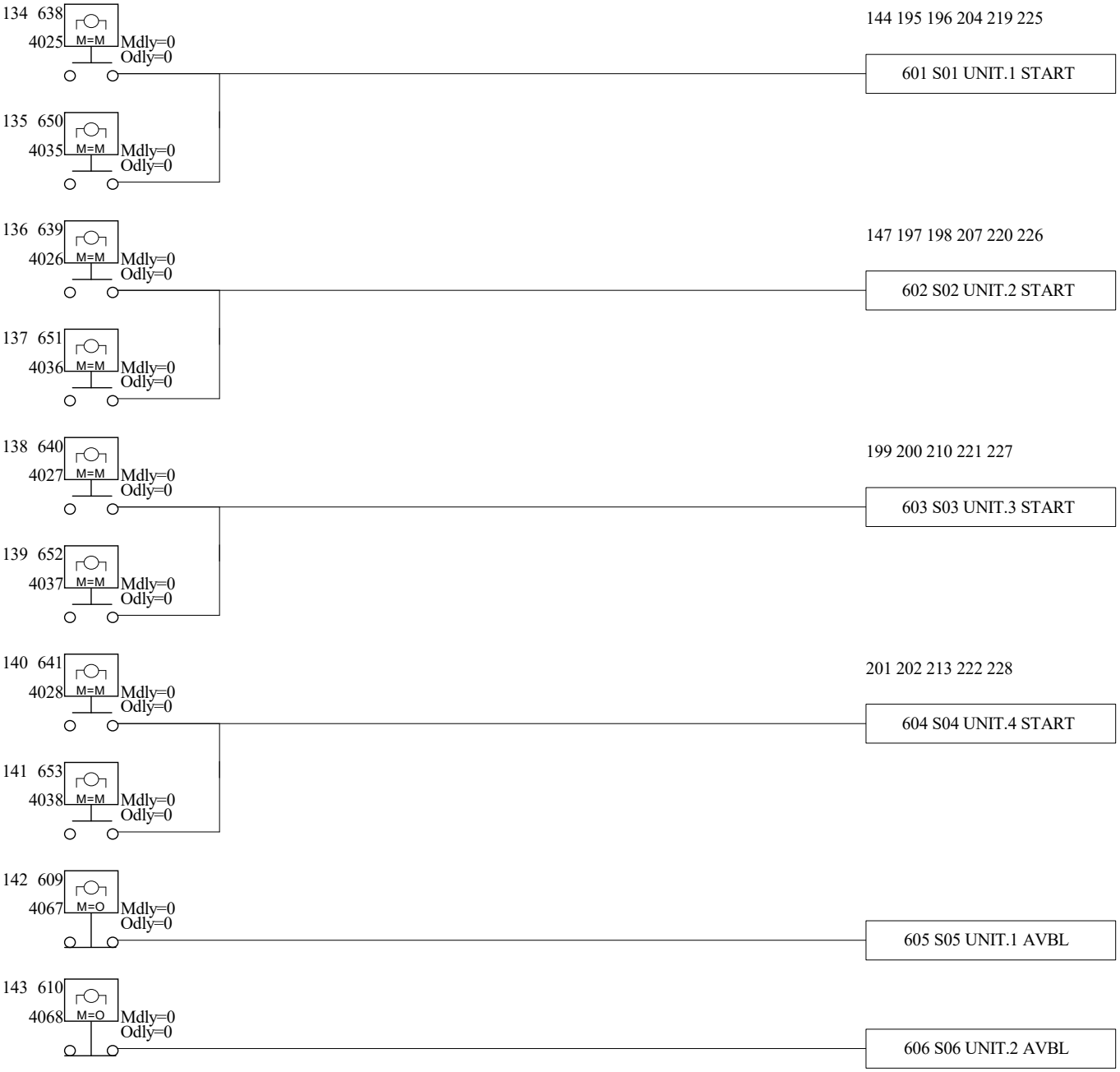
1210 NOTIFICATION
PER TO RUN 2

Logic Diagram MCS_CHLC 1-4 0 0 0

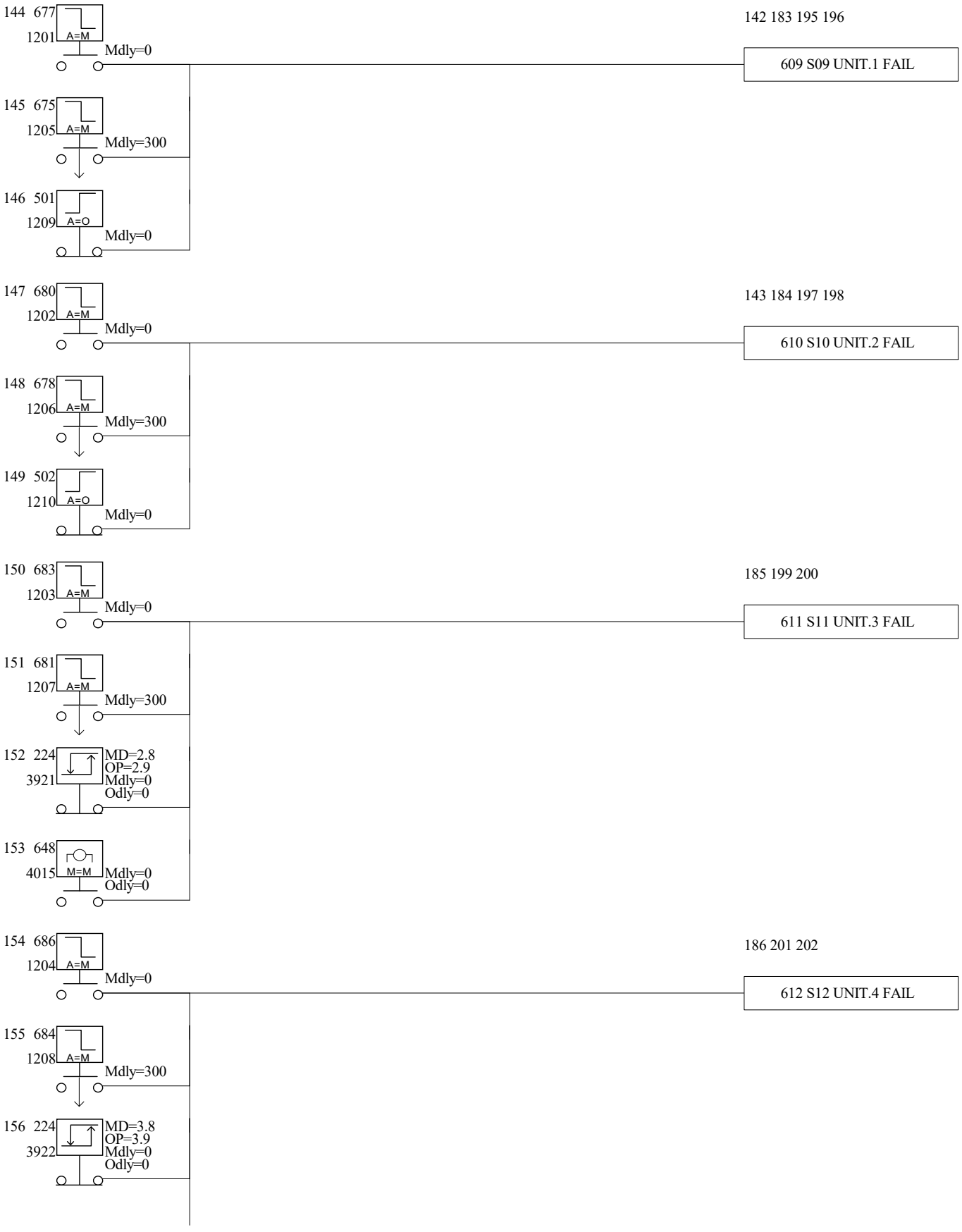
131
Enable when 637 Made
3501 GROUP NO.01
P02 SEQ CNTL2 0.0

132
Enable when 637 Made
3502 GROUP NO.02
P02 SEQ CNTL3 0.0

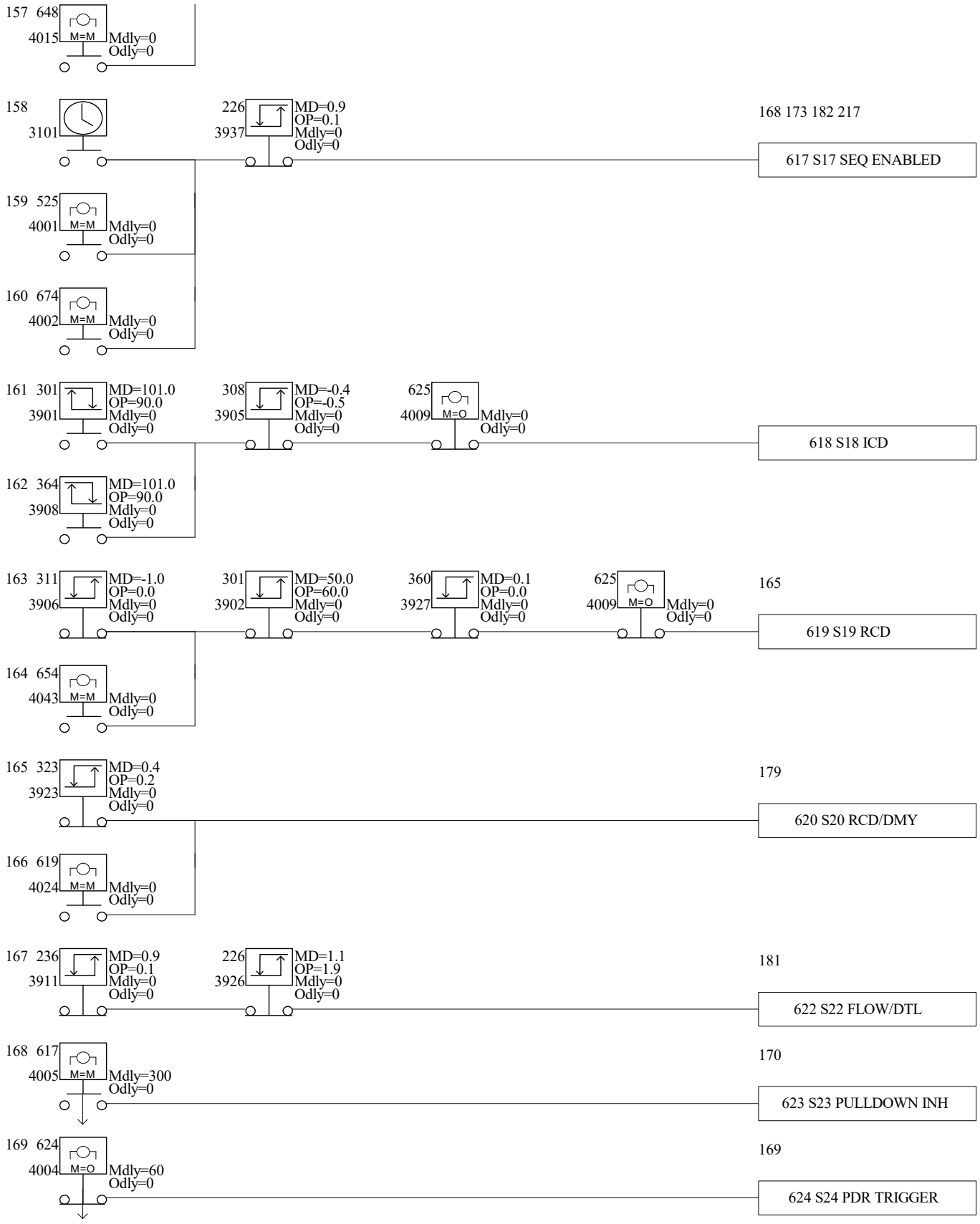
133
Enable when 626 Made
3701 LOOP No.01
P01 S.T.A.3F37 0.0



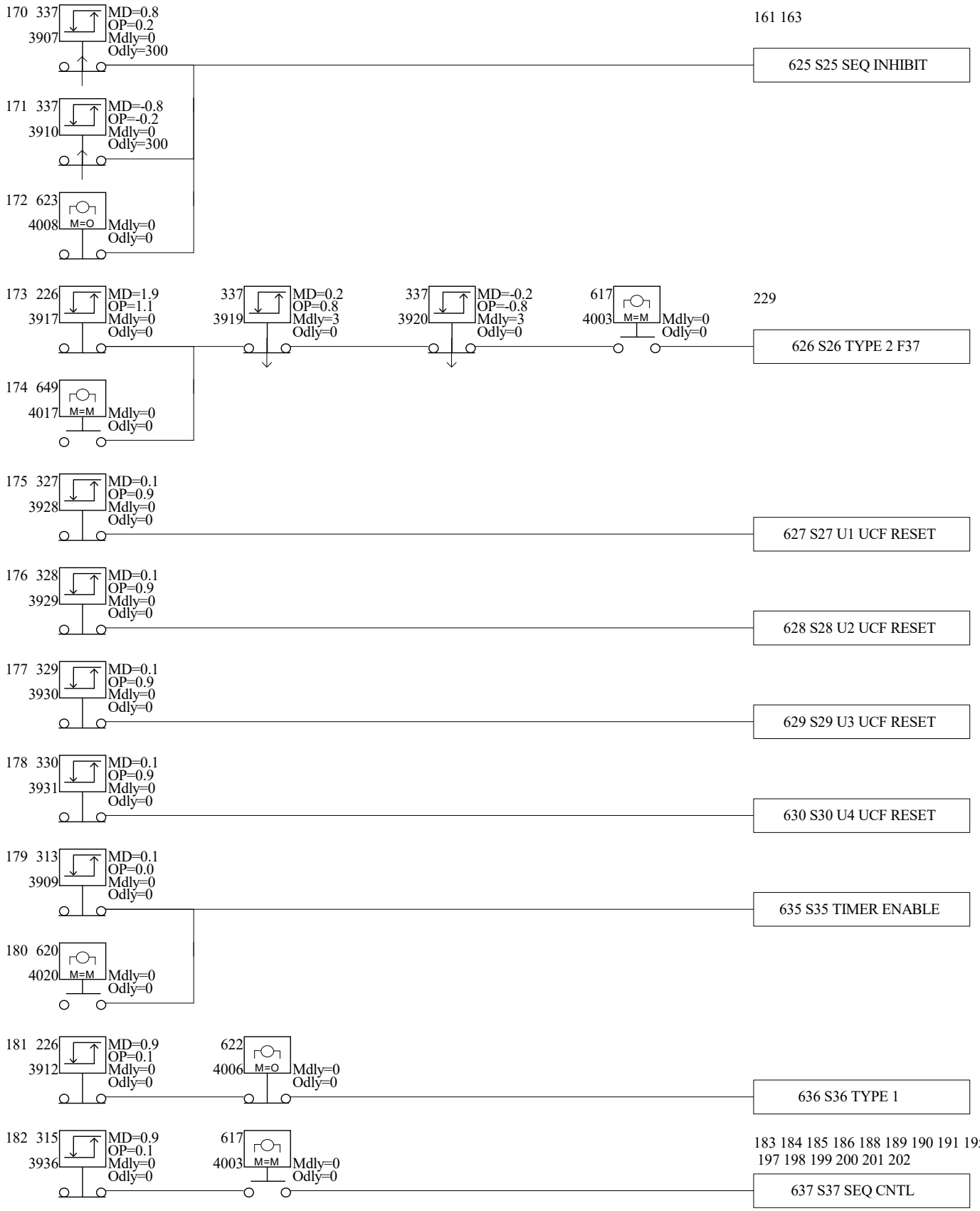
Logic Diagram MCS_CHLC 1-4 0 0 0



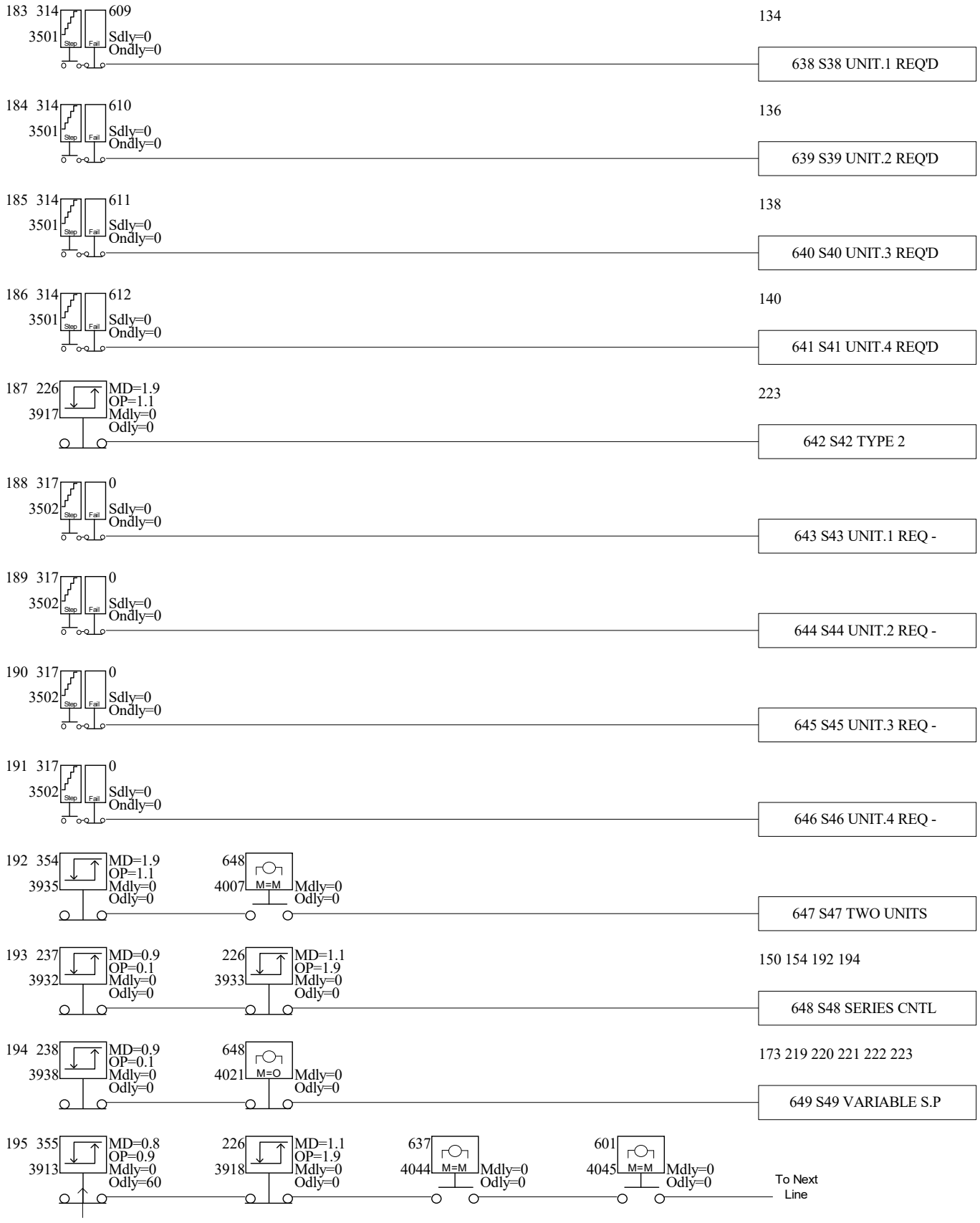
Logic Diagram MCS_CHLC 1-4 0 0 0



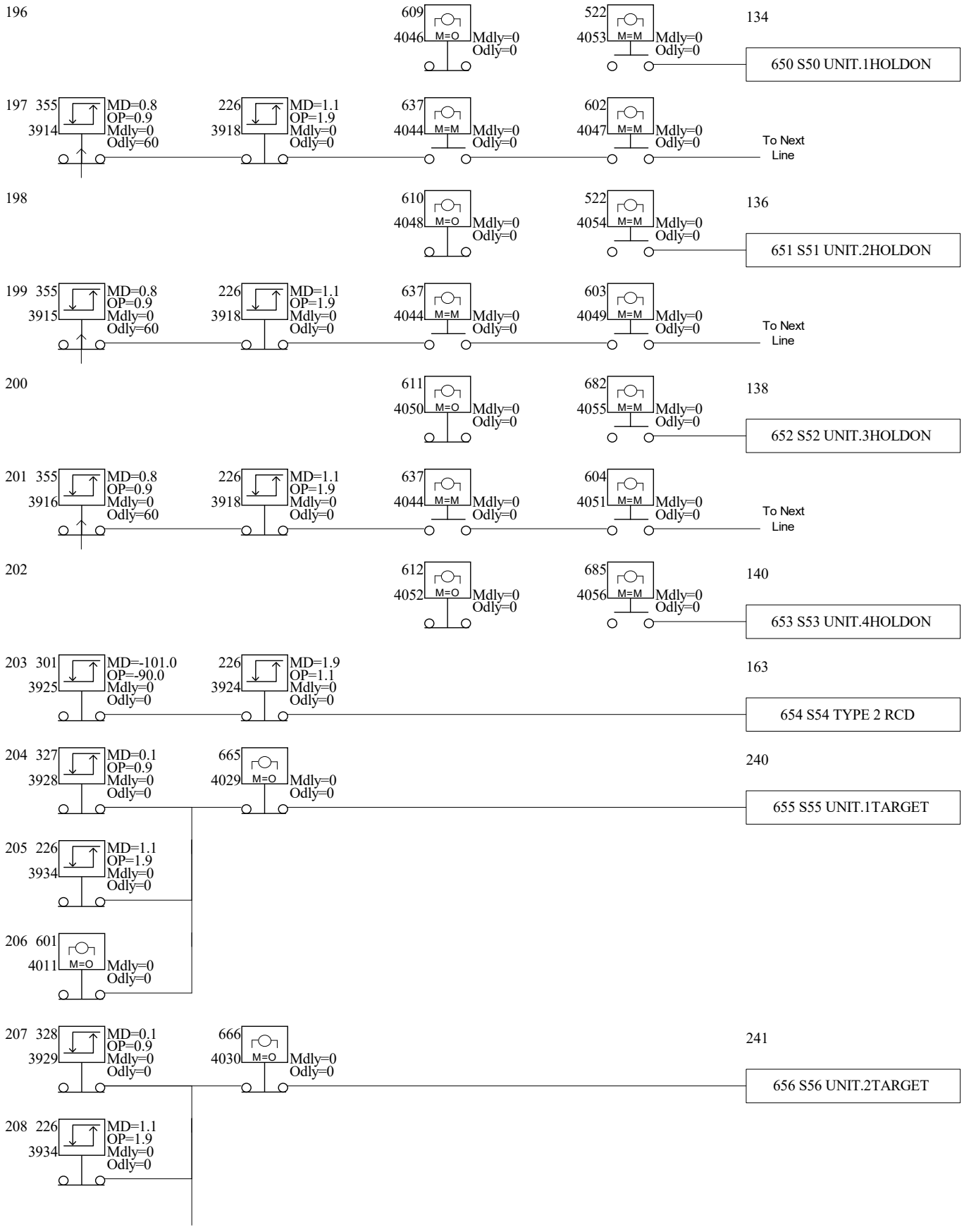
Logic Diagram MCS_CHLC 1-4 0 0 0



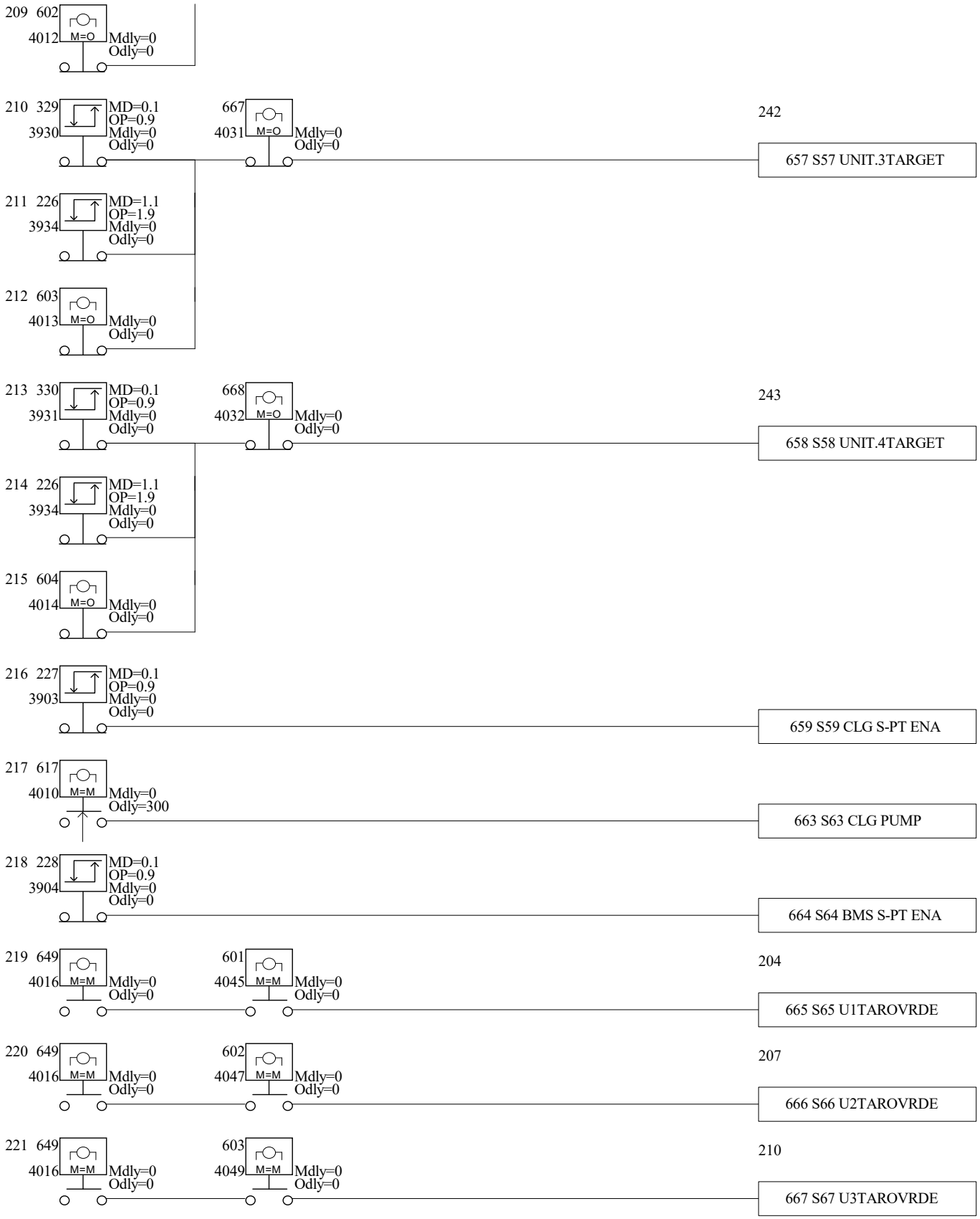
Logic Diagram MCS_CHLC 1-4 0 0 0



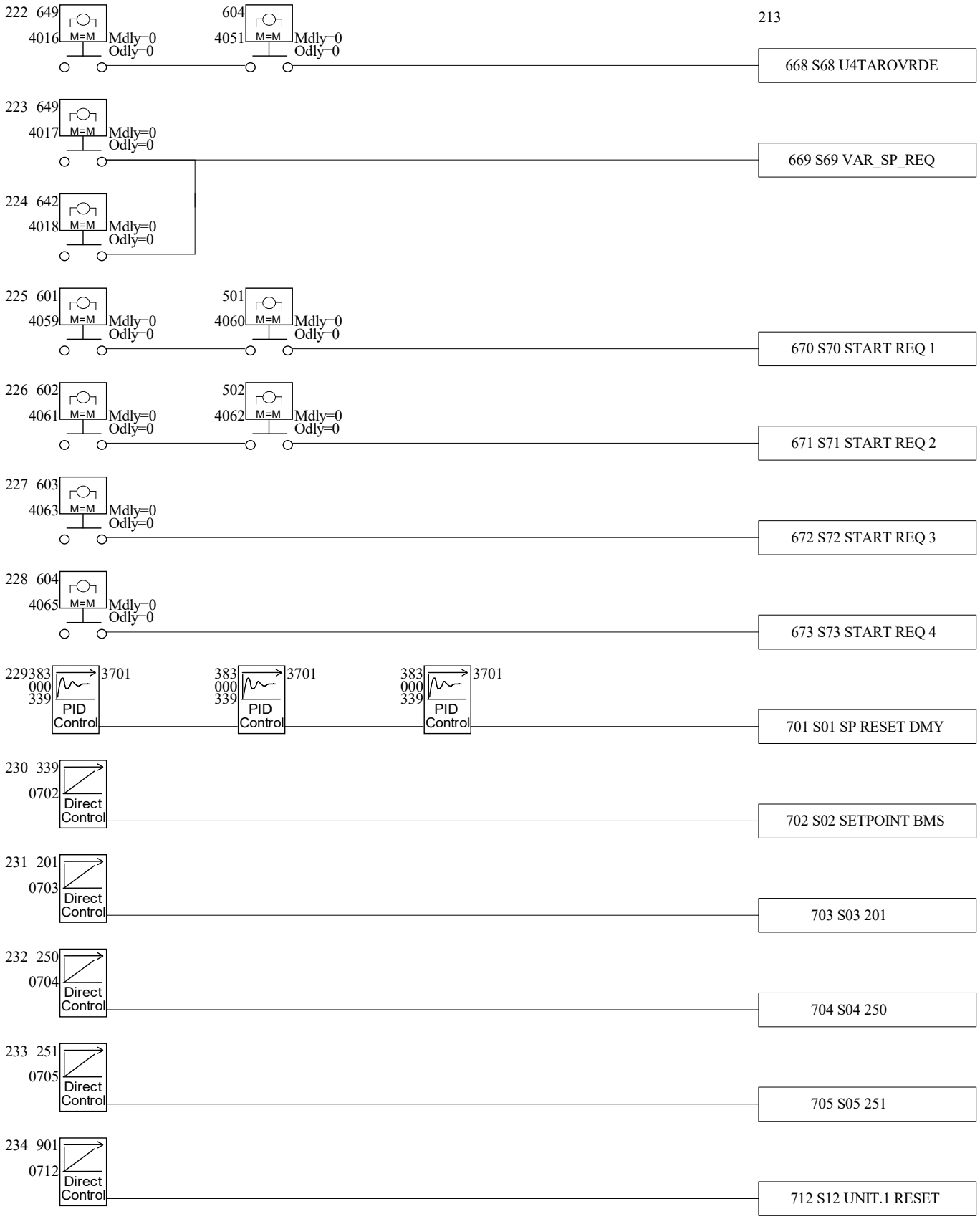
Logic Diagram MCS_CHLC 1-4 0 0 0



Logic Diagram MCS_CHLC 1-4 0 0 0



Logic Diagram MCS_CHLC 1-4 0 0 0



Logic Diagram MCS_CHLC 1-4 0 0 0